REMARKS

This is a supplemental amendment under 37 CFR §1.116. In view of the following comments, applicant respectfully requests an Advisory Action or a Notice of Allowance. The purpose of this amendment is to put the claims in condition for allowance or, alternately, in better form for appeal. The amendments and specific arguments herein, to the extent they were not presented earlier, are now presented because they are necessitated by the arguments made by the Examiner in the last paper. It is submitted that these amendments do not raise new issues and do not require any further searching.

Claims 1-4, 7-8, 10, 12, 17-19, and 22-30 are in this application. Claims 5-6, 9, 11, 13-16, and 20-21 have been cancelled. Claims 4, 7, 10, 17-18, 27, and 30 have been amended.

The Examiner rejected claims 1-3, 16-17, 21, and 26 under 35 U.S.C. §102(b) as being anticipated by or, in the alternative, under 35 U.S.C. §103(a) as being unpatentable over Larson et al. (U.S. Patent No. 5,481,680). As noted above, claims 16 and 21 have been cancelled. For the reasons set forth below, applicant respectfully traverses the rejections of claims 1-3, 17, and 26.

Claim 1 recites:

> "assigning a number of first addresses to a group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits; and
>
> "forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period."

In rejecting the claims, the Examiner pointed to the column of addresses shown in the table of FIG. 7 as constituting the number of first addresses. In the amendment filed on May 15, 2006, applicant noted that claims 1 and 16-17 can not be anticipated by Larson because Larson fails to teach or suggest that a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group. As shown in FIG. 7 of Larson, no device has a grant G0-G3 associated with two consecutive addresses from the column of addresses.

For example, memory address 0001 has been assigned to a first device (CPU 14, DMA 16, DMA 18, or DMA 20) so that when address 0001 is received, the memory outputs grant G0 to the first device. In addition, the next memory address 0010 has been assigned to a second device (CPU 14, DMA 16, DMA 18, or DMA 20) so that when address 0010 is received, the memory outputs grant G1 to the second device. As a result, the consecutive memory addresses 0001 and 0010 are not assigned to the

same device, but instead are assigned to two different devices which respond to grants G0 and G1.

In rejecting claim 1 in the office action mailed on June 28, 2006, the Examiner acknowledged that the Larson reference does not disclose that a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group. In rejecting claims 16-17, the Examiner appears to indicate that the limitation that the logic circuit assign a number of first addresses to the group of devices such that two or more consecutive first addresses are assigned to each device in the group was rejected as in claim 1.

In the after-final paper mailed on August 24, 2006, applicant noted that since the Examiner acknowledged that Larson does not disclose that a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group, claims 1 and 16-17 are not anticipated by the Larson reference. In addition, since claims 2-3 depend either directly or indirectly from claim 1, claims 2-3 are not anticipated by the Larson reference for the same reasons that claim 1 is not anticipated by the Larson reference.

In the Advisory Action, the Examiner argued that the Larson reference taught the "assigning a number of first addresses" element. Specifically, the Examiner pointed to FIG. 1 and the text at column 2, lines 26-56 of Larson as teaching that a range of addresses in the memory device 12 shown in FIG. 1 of Larson is assigned to each of the DMA devices 16, 18, and 20 shown in FIG. 1 of Larson.

Applicant, however, has been unable to find any discussion in Larson that teaches or suggests that two or more consecutive addresses in memory device 12 are assigned to each DMA device 16, 18, and 20. The text cited by the Examiner states

that "DMA devices 16, 18, and 20 directly read and write locations in memory 12 via bus 10." (See column 2, lines 37-38 of Larson.)

Thus, the Larson reference does not teach that two or more consecutive addresses are assigned to each DMA device, but instead merely teaches that each DMA device can directly read from and write to memory device 12. As a result, each DMA device 16, 18, and 20 can potentially read from and write to the same locations in memory 12.

Thus, since the Larson reference does not teach or suggest assigning two or more consecutive addresses from memory device 12 to each DMA device, where no two DMA devices have the same first addresses, claims 1 and 17 are not anticipated by the Larson reference. In addition, since claims 2-3 depend either directly or indirectly from claim 1, claims 2-3 are not anticipated by the Larson reference for the same reasons that claim 1 is not anticipated by the Larson reference.

In addition, applicant has been unable to find any discussion in Larson that teaches or suggests that only consecutive addresses are assigned to each DMA device as required by claim 3. Thus, claim 3 is not anticipated by Larson for this additional reason as well.

Further, even if, for the sake of argument, each DMA device 16, 18, and 20 shown in FIG. 1 of Larson is assigned two or more consecutive first addresses in memory device 12, the Examiner has not pointed to anything that can be read to be the "forming a number of second addresses" element that is also required by claim 1, and the "forms a number of second addresses" limitation of claim 17.

Applicant has been unable to find any discussion in Larson that teaches or suggests that the addresses associated with a DMA device in memory device 12 shown in FIG. 1 of Larson are ever converted into a number of second addresses by

rearranging the "sequence of bits in a plurality of the number of first addresses" as required by claims 1 and 17.

In the June 28, 2006 Office Action, the Examiner appeared to point to the grant bits G0-G3 shown in the table in FIG. 7 as constituting the number of second addresses. Applicant, however, has been unable to find any discussion in Larson that teaches or suggests that the addresses associated with a DMA device in memory device 12 shown in FIG. 1 of Larson are ever converted to form the grant bits shown in the table in FIG. 7 of Larson.

Thus, since the Examiner has not pointed to anything that can be read to be the "forming a number of second addresses" element of claim 1 and the "forms a number of second addresses" limitation of claim 17, claims 1 and 17 are not anticipated by the Larson reference for this further reason. In addition, since claims 2-3 depend either directly or indirectly from claim 1, claims 2-3 are not anticipated by the Larson reference for the same reasons that claim 1 is not anticipated by the Larson reference.

In further rejecting claim 1 in the June 28, 2006 Office Action, the Examiner also pointed to column 5, lines 47-50 of Larson as teaching that, although the block of memory illustrated in FIG. 7 contains a simple priority grant algorithm, the block of memory is not required to contain the priority scheme shown in FIG. 7.

In view of this text, the Examiner argued that Larson teaches that any other arbitration scheme can be used, including one where a number of first addresses are assigned to a group of devices such that two or more consecutive first addresses are assigned to each device in the group and no two devices have the same first address.

In the after-final paper mailed on August 24, 2006, applicant noted that the mere teaching that other arbitration schemes can be used does not render obvious

every other conceivable arbitration scheme. The logical extension of the Examiner's argument is that it is impossible to ever invent another arbitration scheme because all conceivable arbitration schemes are obvious in view of Larson's teaching that another arbitration scheme can be used.

In the Advisory Action, the Examiner argued that since Larson teaches that any other arbitration scheme can be used, it would have been obvious to implement other known arbitration schemes. However, from what can be determined, the Examiner has not pointed to any known arbitration schemes that read on the limitations of the claims. A prima facia case of obviousness requires that the Examiner identify a known arbitration scheme before arguing that it would be obvious to incorporate the teaching from a known arbitration scheme into Larson. Thus, the Examiner has not established a prima facia case of obviousness.

Further, even if, for the sake of argument, the Examiner could point to a prior art arbitration scheme that has two or more consecutive first addresses assigned to each device where no two devices have the same first addresses, a prima facia case of obviousness requires that the Examiner also set forth why one skilled in the art would be motivated to modify Larson in view of a particular known arbitration scheme.

In the Advisory Action, the Examiner stated that assigning a device to have two or more consecutive first addresses would provide a unique range of addresses so the device can be identified based on a given address. However, in the table shown in FIG. 7 of Larson, a unique set of (first) addresses is already associated with each device so the device can be identified based on a given (first) address. One skilled in the art would not be motivated to make a change to Larson to obtain a result that is already provided by Larson.

Further, since the table shown in FIG. 7 of Larson already shows a sequential list of addresses (read to be the number of first addresses) where no device is associated with two or more consecutive addresses, it is unclear how the table in FIG. 7 of Larson would be modified to read onto all of the limitations of the claims.

Thus, since a teaching that other approaches can be used does not render obvious every other conceivable approach, and the Examiner has not established a prima facia case of obviousness, claims 1 and 17 are patentable over Larson. In addition, since claims 2-3 depend either directly or indirectly from claim 1, claims 2-3 are patentable over Larson for the same reasons that claim 1 is patentable over Larson.

With respect to claim 26, in the amendment mailed on May 15, 2006, applicant noted that claim 26 is not anticipated by Larson because Larson fails to teach or suggest that no two second addresses are identical. In the office action mailed on June 28, 2006, the Examiner indicated that claim 26 was rejected on the same rationale and arguments as the rejection of claim 1.

In rejecting claim 1, the Examiner pointed to the rows of addresses shown in the left column of FIG. 7 of the Larson reference as constituting the first addresses required by the claims, and appears to point to the rows of grant bits G0-G3 shown in FIG. 7 of Larson as constituting the second addresses required by the claims.

In the amendment mailed on May 15, 2006, applicant noted that FIG. 7 of the Larson reference teaches that the contents of grant bit rows 2, 4, 6, 8, 10, 12, 14, and 16 are identical, each having the value of 0001. Thus, rather than teaching that no two rows of grant bits are identical, Larson instead teaches that a number of the rows of grant bits are identical. Therefore, since Larson fails to teach or suggest that no

two rows of grant bits are identical, the rows of grant bits can not be read to be the second addresses required by claim 26.

However, from what can be determined, the Examiner did not address this argument in the office action mailed June 28, 2006 or the Advisory Action mailed September 22, 2006. As a result, claim 26 is not anticipated by Larson.

The Examiner objected to claims 4, 7-8, 10, 12, 18-19, and 27-30, but indicated that these claims would be allowable if amended to be in independent format to include all of the limitations of the base claim and any intervening claims. Claims 4, 7, 10, 18, and 27 have been amended to be in independent format, and are believed to include all of the limitations of the base claim and any intervening claims. Claims 8, 12, 19, and 28-29 have not been amended as these claims depend from claims 7, 10, 18, and 27, respectively. In addition, claim 30 has been amended to depend from claim 27.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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